said semiconductor chip;

a plurality of conductors being disposed on said one surface of said substrate to surround said semiconductor chip along the four sides thereof, said conductors being arranged so as to extend with one respective end thereof in a radial pattern toward said semiconductor chip;

a plurality of bonding wires electrically connecting said bonding pads with tips of said conductors respectively; and

a resin body sealing said semiconductor chip and said plurality of bonding wires;

wherein said bonding pads include first adjacent bonding pads disposed at each of four corners defined by the four sides of said main surface of said semiconductor chip and second adjacent bonding pads disposed at areas of the four sides of said semiconductor chip which are farther from the four corners than said first adjacent bonding pads; and

wherein a pitch between said first adjacent bonding pads is wider than a pitch between said second adjacent bonding pads.

REMARKS

By the above amendment, the status of the parent application has been updated, a typographical error in the specification has been corrected and independent claims 1, 7 and 12 have been amended to more particularly recite the arrangement of the conductors as illustrated in Fig. 1 of the drawings of this application, for example.

In accordance with the present invention, as illustrated in Fig. 1, for example, the plurality of conductors 4 are arranged with respect to the semiconductor chip 2 so as to surround the semiconductor chip along the four sides with the conductors 4 including the ends or tips of the conductors proximate to the semiconductor chip

extending in a radial pattern toward the semiconductor chip. Applicants note that as described in the specification of this application, the arrangement of the conductors and the arrangement of the bonding pads on the semiconductor chip in the manner defined in each of independent claims 1, 7 and 12 enable connection of the conductors and pads without short-circuiting of wires in the case of using wire-bonding, for example. That is, since the conductors or leads 4, as illustrated in Fig. 1, for example, which are to be wire-bonded are disposed on (or fixed on) the surface of the substrate in the radial pattern, so as to radially surround the semiconductor chip without the requirement for suspending leads at the vicinity of the four corners of the chip, plural number of conductors or leads can be arranged at the periphery of the chip at the same time, since in accordance with the present invention, the bonding pads of the semiconductor chip are arranged such that a pitch of adjacent bonding pads in the vicinity of the four corners is greater than a pitch of adjacent bonding pads at other positions along the sides of the semiconductor chip. With the disclosed construction, a highly reliable semiconductor device is obtained. Applicants submit that the aforementioned features are now clearly recited in independent claims 1, 7 and 12 and therewith the dependent claims, and that such features are not disclosed or taught in the cited art, as it will become clear from the following discussion.

The rejection of claims 1-16 under 35 U.S.C. 103(a) as being unpatentable over Ishikawa et al (US Patent 5,907,190) in view of Japanese Patent 59105349 to Mori et al, is traversed insofar as it is applicable to the present claims, and reconsideration and withdrawal of the rejection are respectfully requested.

With regard to the requirements to support a rejection under 35 U.S.C. 103, reference is made to the decision of In re Fine, 5 USPQ 2d 1596 (Fed. Cir. 1988), wherein the court pointed out that the PTO has the burden under §103 to establish a prima facie case of obviousness and can satisfy this burden only by showing some

objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. As noted by the court, whether a particular combination might be "obvious to try" is not a legitimate test of patentability and obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. As further noted by the court, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.

Furthermore, such requirements have been clarified in the recent decision of In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002) wherein the court in reversing an obviousness rejection indicated that deficiencies of the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge". The court pointed out:

> The Examiner's conclusory statements that "the demonstration mode is just a programmable feature which can be used in many different device[s] for providing automatic introduction by adding the proper programming software" and that "another motivation would be that the automatic demonstration mode is user friendly and it functions as a tutorial" do not adequately address the issue of motivation to combine. This factual question of motivation is immaterial to patentability, and could not be resolved on subjected belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher."... Thus, the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion. (emphasis added)

In setting forth the rejection, the Examiner recognizes that Ishikawa et al does not disclose a pitch between adjacent bonding pads increases in a direction toward four corners defined by the four sides of the main surface of the chip. The Examiner

contends that the Japanese patent discloses such feature regarding the pitch of bonding pads. The Examiner therefore concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to increase the pitch toward the corner of the chip in Ishikawa's invention in order to have constant wire (conductor) intervals.

Irrespective of the position set forth by the Examiner, applicants submit that neither Ishikawa et al nor the Japanese patent disclose or teach the claimed features as now recited in independent claims 1, 7 and 12 with the Japanese patent to Mori et al specifically disclosing an arrangement of the conductors different from that recited in the claims. Turning to Ishikawa et al, although the Examiner contends that this patent discloses "a plurality of conductors 5 surrounding the chip", Ishikawa et al only discloses cross sectional views and therefore only discloses conductors 5 being arranged with respect to two sides of the chip with bonding pads being disposed along the two sides. Thus, applicants submit that Ishikawa et al, contrary to the contentions of the Examiner, fails to disclose bonding pads being disposed along four sides of the main surface of the semiconductor chip as well as a plurality of conductors being disposed on the one surface of the substrate to surround the semiconductor chip along the four sides thereof. Furthermore, in addition to such deficiency of Ishikawa et al and the other deficiency thereof as recognized by the Examiner, applicants submit that there is no disclosure or teaching in Ishikawa et al of the conductors being arranged so as to extend with one respective end thereof in a radial pattern toward the semiconductor chip. As such, applicants submit that each of independent claims 1, 7 and 12 patentably distinguish over Ishikawa et al in the sense of 35 U.S.C. 103 and should be considered allowable thereover.

With respect to the Japanese patent to Mori et al, assuming arguendo that this reference discloses a quadrilateral shaped chip with conductors b arranged along the four sides thereof and bonding pads d, it is readily apparent that the

conductors or leads b as illustrated in Fig. 1 of this reference extend in a perpendicular pattern to a respective side of the chip. Thus, the disclosure of the Japanese patent to Mori et al is contrary to the claimed features of independent claims 1, 7 and 12 that the conductors are arranged so as to extend with one respective end thereof in a radial pattern toward the semiconductor chip. As such, applicants submit that independent claims 1, 7 and 12 patentably distinguish over the Japanese patent to Mori et al in the sense of 35 U.S.C. 103 and such Japanese patent does not overcome the deficiencies of Ishikawa et al, such that the combination fails to provide the claimed features as set forth in independent claims 1, 7 and 12 and the dependent claims of this application. Accordingly, applicants submit that all claims patentably distinguish over this proposed combination of references in the sense of 35 U.S.C. 103 and should be considered allowable thereover.

As to the arrangement of conductors as disclosed and claimed in this application, applicants note that the reference to Davies et al, cited and not applied in rejecting claims of this application, also does not provide an arrangement of conductors as defined in that as illustrated, the portions of the conductors 13 as illustrated in Fig. 1A of the drawings of this application, have one respective end thereof arranged to extend perpendicular to a respective side of the semiconductor chip, as is provided in the Japanese patent to Mori et al rather than a radial pattern arrangement as now recited in the independent claims of this application.

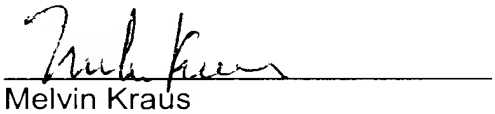
As to the dependent claims, applicants note that irrespective of the Examiner's contentions concerning what is considered to be obvious and what is well known in the art, applicants note that the decision of In re Lee, supra clearly points to the inappropriateness of utilizing such analysis to support a rejection under 35 U.S.C. 103. Thus, applicants submit that the dependent claims recite further features not disclosed or taught in the cited art, and patentably distinguish over the

cited art in the sense of 35 U.S.C. 103, and should be considered allowable thereover.

In view of the above amendments and remarks, applicants submit that all claims present in this application should now be in condition for allowance, and issuance of an action of a favorable nature is courteously solicited.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (501.35250CX3) and please credit any excess fees to such deposit account.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 1, please amend the paragraph beginning at line 4 as follows:

CROSS REFERENCE TO RELATED APPLICATION

This is a continuation of U.S. application Serial No. 08/820,228, filed March 18, 1997, now U.S. Patent No. 6,265,762, the subject matter of which is incorporated by reference herein.

Page 15, please amend the paragraph beginning at line 5 as follows:

The bonding for connecting the pad electrodes 11 to the points of the inner leads 4 is effected by the wires 13, but the ~~cap~~ pad pitch is made wider in the arrangement in the pad electrodes 11 as one gets near the corner. Accordingly, it is possible to prevent the wires 13 at the corner portion from coming into contact with adjacent wires 13 to thereby produce a short-circuit even when the wire 13 is transformed by the occurrence of wire running or the like. As an example, an Au fine wire or the like having a diameter of approximately 25 μm to 35 μm is used as the bonding wire 13.

IN THE CLAIMS:

Please amend claims 1, 7 and 12 as follows:

1. (amended) A semiconductor device comprising:

a substrate;

a semiconductor chip mounted on one surface of said substrate, said semiconductor chip having an integrated circuit and bonding pads formed on a main surface thereof, said main surface of said semiconductor chip having a quadrilateral shape, said bonding pads being disposed along four sides of said main surface of said semiconductor chip;

a plurality of conductors being disposed on said one surface of said substrate to surround said semiconductor chip along the four sides thereof, said plurality of conductors being arranged so as to extend with one respective end thereof in a radial pattern toward said semiconductor chip;

a plurality of bonding wires electrically connecting said bonding pads with tips of said plurality of conductors, respectively; and

a resin body sealing said semiconductor chip, said plurality of conductors and said plurality of bonding wires;

wherein a pitch between adjacent bonding pads increases in a direction toward four corners defined by the four sides of said main surface of said semiconductor chip.

7. (amended) A semiconductor device comprising:

a substrate;

a semiconductor chip mounted on one surface of said substrate, said semiconductor chip having an integrated circuit and bonding pads formed on a main surface thereof, said main surface of said semiconductor chip having a quadrilateral shape, said bonding pads being disposed along four sides of said main surface of said semiconductor chip;

a plurality of conductors being disposed on said one surface of said substrate to surround said semiconductor chip along the four sides thereof, said conductors being arranged so as to extend with one respective end thereof in a radial pattern toward said semiconductor chip;

a plurality of bonding wires electrically connecting said bonding pads with tips of said conductors respectively; and

a resin body sealing said semiconductor chip and said plurality of bonding wires;

wherein a pitch between first ones of adjacent bonding pads at each of four corners defined by the four sides of said main surface of said semiconductor chip is

wider than a pitch between second ones of adjacent bonding pads which are disposed at other than the four corners and at a relatively central position of each of the four sides.

12. (amended) A semiconductor device comprising;

a substrate;

a semiconductor chip mounted on one surface of said substrate, said semiconductor chip having an integrated circuit and bonding pads formed on a main surface thereof, said main surface of said semiconductor chip having a quadrilateral shape, said bonding pads being disposed along four sides of said main surface of said semiconductor chip;

a plurality of conductors being disposed on said one surface of said substrate to surround said semiconductor chip along the four sides thereof, said conductors being arranged so as to extend with one respective end thereof in a radial pattern toward said semiconductor chip;

a plurality of bonding wires electrically connecting said bonding pads with tips of said conductors respectively; and

a resin body sealing said semiconductor chip and said plurality of bonding wires;

wherein said bonding pads include first adjacent bonding pads disposed at each of four corners defined by the four sides of said main surface of said semiconductor chip and second adjacent bonding pads disposed at areas of the four sides of said semiconductor chip which are farther from the four corners than said first adjacent bonding pads; and

wherein a pitch between said first adjacent bonding pads is wider than a pitch between said second adjacent bonding pads.